What is Claimed is:

[c1] A method of testing a DRAM, the DRAM comprised of a multiplicity of DRAM blocks, comprising:

in a processor based built-in self test system, generating a test data pattern;

for each DRAM block, performing a write of said test data pattern into said DRAM block, performing a pause for a predetermined period of time, and performing a read of a resulting data pattern from said DRAM block;

wherein for each DRAM block, said performing said write of said test pattern into said DRAM block is performed before said performing said pause for said predetermined period of time, and said performing said read of said resulting data pattern from said DRAM block is performed after said performing said pause for said predetermined period of time; and

wherein at least a portion of said pause for said predetermined period of time of two or more said DRAM blocks overlap in time.

[c2] The method of claim 1, wherein said step of performing said write of said test pattern into said DRAM is performed simultaneously for all said DRAM blocks of said DRAM.

[c3] The method of claim 1, wherein said step of performing said write of said test pattern into said DRAM block is performed sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks, the writing of a previous DRAM block of said multiplicity of DRAM blocks being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM blocks.

[c4] The method of claim 1, wherein said step of performing a pause for said predetermined period of time is performed simultaneously for all said DRAM blocks of said DRAM.

[c5] The method of claim 1, wherein at least a portion of said pause for said predetermined period of time of at least one of said DRAM blocks of said DRAM overlaps in time said step of writing of said test pattern into at least one other

DRAM block of said DRAM.

[c6] The method of claim 1, wherein said step of performing said read of said resulting pattern into said DRAM block is performed sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks, the reading of any previous DRAM block of said multiplicity of DRAM blocks being completed before the reading of a subsequent DRAM block of said multiplicity of DRAM blocks.

[c7] The method of claim 1, further including:

for each DRAM block, determining redundancy allocation information based on said resulting data pattern; and

storing said redundancy allocation information for each said DRAM in separate registers, the storing of any previous redundancy allocation information for a previous DRAM block of said multiplicity of DRAM blocks being completed before the storing of subsequent redundancy information for a subsequent DRAM block of said multiplicity of said DRAM blocks.

[c8] The method of claim 7, wherein the number of said registers is equal to the number of said DRAM blocks.

[c9] The method of claim 7, wherein said registers are coupled in series and further including scanning out each register sequentially.

[c10] The method of claim 7, further including:

writing back fuse delete information based on said redundancy allocation information into said registers.

[c11] A processor based built-in self test system for testing an embedded DRAM, said embedded DRAM including a multiplicity of DRAM blocks, each DRAM block comprising a multiplicity of wordlines and bitlines, comprising:

means for generating a test data pattern;

means for writing said test data pattern into each DRAM block simultaneously;

means for reading out a resultant data pattern from each said DRAM

block after a predetermined period of time has elapsed from said writing of said test data into each said DRAM block, said reading out occurring sequentially from a first DRAM block to a last DRAM block of said multiplicity of said DRAM blocks, the reading of any previous DRAM block of said multiplicity of DRAM blocks being completed before the reading of a subsequent DRAM block of said multiplicity of DRAM blocks;

means for storing scan out data for each said DRAM block on a register, said scan out data comprising said resultant data pattern or information based on said resultant data pattern of each said DRAM block; and

means for scanning out said scan out data, the scanning out of any previous scan out data for a previous DRAM block of said multiplicity of DRAM blocks is completed before the scanning in of scan out data for a subsequent DRAM block of said multiplicity of DRAM blocks.

[c12] The test system of claim 11, further including:

means for comparing said resultant data pattern with said test data pattern and for creating redundancy allocation information based on the comparison between said resultant data pattern and said test data pattern; and

wherein said scan out data comprises said redundancy allocation information.

[c13] A processor based built-in self test system for testing an embedded DRAM, said embedded DRAM including a multiplicity of DRAM blocks, each DRAM block comprising a multiplicity of wordlines and bitlines, comprising:

means for generating a test data pattern;

means for writing said test data pattern into each DRAM block sequentially from a first DRAM block to a last DRAM block of said multiplicity of DRAM blocks, the writing of a previous DRAM block being completed before the writing of a subsequent DRAM block of said multiplicity of DRAM blocks;

means for reading out a resultant data pattern from each said DRAM block after a predetermined period of time has elapsed from said writing of said test data into each said DRAM block, said reading out occurring

sequentially from a first DRAM block to a last DRAM block of said multiplicity of said DRAM blocks, the reading of any previous DRAM block of said multiplicity of DRAM blocks being completed before the reading of a subsequent DRAM block of said multiplicity of DRAM blocks;

means for storing scan out data for each said DRAM block on a different store register of a multiplicity of store registers, said scan out data comprising said resultant data pattern or information based on said resultant data pattern of each said DRAM block, the storing of scan out data for a previous DRAM block of said multiplicity of DRAM blocks being completed before the storing of scan out data for a subsequent DRAM block of said multiplicity of said DRAM blocks.

[c14] The test system of claim 13, further including means for scanning out said scan out data from said multiplicity of store registers sequentially, the scanning out of any scan out data of a previous store register of said multiplicity of store registers being completed before the scanning out of scan out data of a subsequent store register of said multiplicity of store registers.

[c15] The test system of claim 13, wherein the number of said store registers is equal to the number of said DRAM blocks.

[c16] The test system of claim 13, further including:

means for comparing said resultant data pattern with said test data pattern and for creating redundancy allocation information based on the comparison between said resultant data pattern and said test data pattern; and

wherein said scan out data comprises said redundancy allocation information.

[c17] The test system of claim 16, further including means for writing back fuse delete information based on said redundancy allocation information into said multiplicity of store registers.

[c18] The test system of claim 16, which further includes a redundancy allocation register coupled to a redundancy allocation store device, said redundancy allocation store device including an interface shift register coupled to each said

store register of said multiplicity of store registers.

[c19] The test system of claim 18, wherein the state of latches within said redundancy allocation register is simultaneously swapped with the state of latches within said interface shift register.

[c20] The test system of claim 18, wherein the contents of said interface register is written into a previous store register of said multiplicity of store registers as the contents of a subsequent store register of said multiplicity of store registers are simultaneously written into said interface register.